Investigation of Inductance effects reduction in IR drop analysis using diagonal power routing in Power grid circuits in VLSI

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Abstract :
This paper proposes to analyze the IR Drop analysis with the diagonal power grid for either static or dynamic .In high performance digital circuits, clocks are running at high frequencies and it induces the IR drop. Such phenomena can occur on clock lines and long buses. In addition, the switching noise due to inductive voltage drops is an issue for power distribution network in VLSI circuits. The power supply noise mainly manifests itself as a voltage drop in the power distribution networks. The inductance effects can no longer be ignored as technology scaling progresses into sub-nm processes, since interconnect lengths become longer as the functionalities of the IC chip grow. The chip operating frequencies increases into multi-gigahertz range, and signal rise and fall times become faster. Therefore, it is important to model inductive effects accurately for high speed VLSI designs. In this we implemented the Diagonal power routing in top power layer (M9), which reduce the resistance and Inductance (Ldi/dt) effect compared to the orthogonal power grid.

Keywords:diagonal,orthogonal,Ldi/dt,dynamicpower, staticpower, ,electromigration**.**

Introduction: : Advances in CMOS process technology towards 45-20 nm with reducing chip dimensions and increasing frequency requirements, IR drop is fast becoming a dominant factor in determining the chip frequency. In high-performance IC's, the number of switching digital gates is continually increasing, so the current peaks become more important Power Distribution Networks in High Speed Integrated Circuits[1],. Indeed, the combination of several hundred thousands of gates synchronized to the clock leads to huge current glitches. In the same manner, with the shrinking of the technology, the switching currents rise time becomes faster. In conclusion, the factor di/dt can become very important and in induced power supply voltage variation[4]. The electromagnetic field, created by current loops and voltage drops, is then transmitted to its environment by antennas. In ICs, the bonding interconnections and package lead frame both behave as miniature antennas. Indeed, they work like unintentional magnetic and electric dipoles. Finally, unintentional or intentional receivers are able to get the electromagnetic interferences created by the IC's/micro controller. Due to on-chip IR drop, the voltage available across standard cells' supply rails is less than the power-supply voltage resulting into lesser drive current capability and therefore slower switching speeds. Worse, chip might not work at all due to hold violations, if due care is not taken in estimating the clock tree delays accurately with a given IR drop. This problem is hard to solve, as the voltage available at any spatial point in the chip is time varying and is dependent on the state of rest of the circuit. For making absolutely sure that the chip will function in all the use scenarios, it is suggested to perform static and dynamic IR drop analysis coupled with timing analysis for all possible cases Power integrity and energy aware floorplanning[2],. With the advanced technology one of the main challenges facing the chip designers is signal Integrity, IR drop and Electro Migration. With increasing operating frequencies and elevating power consumptions in VLSI circuits, the design and analysis of on chip power distribution networks has become a critical design task. Aggressive interconnect scaling has increased the average current density and the resistance per unit length of wires and on-chip Inductance Power supply noise aware and decoupling capacitance placement[5]. Since the supply voltage level is also reduced with the technology scaling, the power supply noise becomes even more pronounced because the ratio of the peak noise voltage to the ideal supply voltage level increases with each scaled technology node. The power supply noise mainly manifests itself as a voltage drop in the power distribution networks.In this we implemented the Diagonal power routing in top power layer (M9) , which reduce the resistance and Inductance effect compared to the orthogonal power grid. The effects of chip temperature, electro migration and interconnect technology scaling are considered during this analysis. The voltage drop effect in the power/ground (P/G) distribution network increases rapidly with technology scaling, and that using well-known countermeasures such as wire-sizing and/or decoupling capacitor insertion Decoupling capacitor planning and sizing for noise and leakage reduction[7],which are typically used in the present design methodologies may be insufficient to limit the voltage fluctuations over the power grid for future technologies. Static analysis is based on resistive value of the power/ground network and does not consider impact of capacitance (intrinsic or intentional). Effective use of capacitance can protect

the dynamic hot spots in the design. However if not used effectively, they can impact total leakage of design. Static analysis does not consider the impact of on-chip LdI/dt inductive or LC resonance noise and off-chip package RLC. So we need to analyze the IR drop and EM analysis to find the regions, implement the methodologies to reduce the IR and EM effects. As power continues to drop with the VLSI technology scaling associated with significance increasing device numbers in a die, power network design becomes a very challenging task for a chip with millions of transistors. The common task in VLSI power network design is to provide enough power lines across the chip to reduce the voltage drops from the power pads to the center of the chip.

Related to work

The voltage drops are mainly caused by the esistance or inductance of the power network metal lines .The power network can be modeled as a low-pass filter with RL segments in series, attached with capacitors at each end. The current sources of the switching gates and the intentional decoupling capacitors are also inserted in the model. The IR drop is roportional to the average current consumed by the circuit in the chip. The L. di/dt drop is proportional to the time-domain change of the current, due to the switching of the logic gates in the chip operation. Because of the large voltage drop due to various factors we need to analyze the IR drop of the power network. The potential sources of power-grid network design problems related to IR drop, ground bounce, and electro migration, and discusses the methodologies available to detect them .Internally reduce the Electromagnetic interference effects in inductance to reduce the IR drop in my research . Integrated-circuit design usually assumes the availability of an ideal power supply that can instantly deliver any amount of current to maintain the specified voltage throughout the chip.The rest of paper organized as follows:The power grid model is described and concepts of IR drop and effective methods to reduce power in circuits in section2.To implement the related procedure for power grid analysis with schematics of static and dynamic,in section3, Experimental results are provided in section 4, To examine the Static and Dynamic power diagonal analysis and electro migration analysis results and discussions in section 5. Finally, concluded.

2.1.BACK GROUND

2.1 IR DROP

IR drop a second-order effect that in ultra deep submicron, with lower supply voltages yielding smaller noise margins, IR drop is a first-order effect and can no longer be ignored during the design process.IR drop is a dynamic phenomenon due primarily to simultaneous switching events in a chip such as clocks, bus drivers, and memory decoder drivers. As large drivers begin to switch, the simultaneous demand for current from the power grid stresses the grid. In a static context, voltage drops are highest near the center of a design and lowest near VDD connections to the power supply. However, during dynamic operation, these simultaneous switching events can cause severe voltage drops anywhere on the chip, and these are the ones that must be identified. These events, usually well known, can be triggered with typically fewer than 100 vectors.Ground bounce is an increase in voltage that occurs on ground networks (VSS or GND) in integrated circuits. The current that is sourced onto the ground network combined with a finite resistance of the ground network leads to localized increases in the ground voltages around the chip. As with IR drop, these increases in the ground voltage also decrease

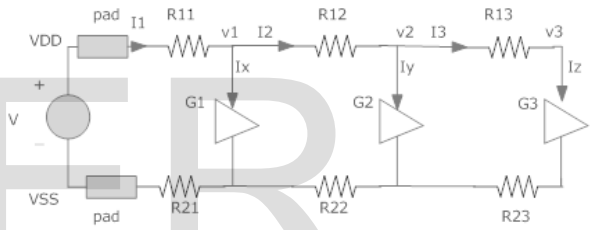

Figure 1 Electrical network representation of the Power grid

the operating voltage of the chip, resulting in the same potential timing problems and functional failures. Validating that the ground voltage does not rise above a 10% noise budget is as important as ensuring that VDD does not drop below a 10% budget. Measuring ground bounce requires that the substrate be modeled as a distributed RC network in parallel with the metal routing for the ground grid. This significantly increases the complexity of the network, especially when pin inductance or a more complicated pin model is included. A limited form of ground bounce could be obtained by modeling substrate contacts as individual ideal capacitances, but these values are difficult to obtain. An even more conservative approach to ground bounce analysis ignores the substrate entirely; however, using this approach, you would see that the behavior observed during analysis would be worse than the actual ground bounce on the chip.The Fig 1. Shows the entire chip power grid is represented in a electrical network with R and C .It shows a chip power supply connected to the chip pads. The power-grid network is illustrated by the R11-R13 resistors for VDD and

R21-R23 resistors for VSS. These resistors represent the resistance of interconnect from the pads to the cells or transistors. G1- G3 cells are connected to VDD and VSS. When we perform transistor or gate-level simulation, the voltages (V1- V3) are typically assumed to be equal. It is further assumed that all power-grid resistances are zero ohms and that all chip components receive ideal power supply voltages. In reality, the power-grid resistances of a chip cannot be ignored. For example, cell G3 never has an ideal VDD voltage at its VDD pin when it is active; it has a lower voltage because the current flowing from the VDD pad to G3 must flow through resistances R11-R13.Ohm's law states that a current, I, flowing through an effective resistance, R, introduces a voltage drop, as given by the equation V =IR. Similarly, cell G3 never has an ideal VSS at its ground pin, because the current flowing from G3 back to the VSS pad must also travel through the ground network resistances R21- R23. In this cause less G3 has an increased voltage at its ground pin. Figure also illustrates the complexity of power grids and IR drop.

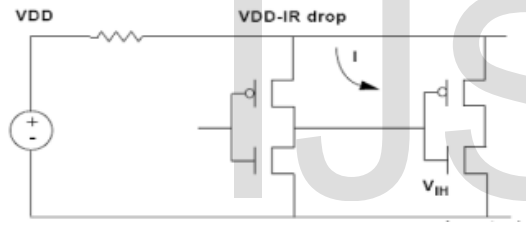

Figure 2 voltage drop in circuit

Experiments have shown that a 5 percent IR drop on a clock buffer can slow down its speed by up to 15 percent. The reduction in speed is due to two mechanisms as shown in fig 2. First, the IR drop on the power input of inverter1 slows the charging rate of the output. The output voltage of inverter1 rises only up to VDD minus the IR drop. In turn, this drop reduces the logical high input voltage (VIH) to inverter2, reducing its switching speed as well.

Two problems have resulted from the traditional approach to working around potential IR drop problems:

1. Timing libraries are constructed on the basis of assumptions about certain amount of IR drop, such as 10 percent. These assumptions add to the timing margins applied to the design. The added margins are becoming quite significant and impede timing closure. As a result, the final chip timing is increasingly predictable. Chips can fail because the IR drop was actually higher, or they can operate at twice their specified frequency

.2. Power grids are heavily over designed. These grids remove a significant amount of chip area from use for signal routing and may result in larger chips.

2.2 Power Grid Analysis Methodologies

The power dissipation in the design is two categories: Static power and Dynamic power

2.2 .1 Static power

Static Power is due to leakage current or other current drawn continuously from the power supply, when the circuit is not switching. It has following components – Power due to Drain Leakage Currents – Power due to Sub Threshold Currents The diode leakage current occurs from the source or drain to the substrate through the reverse-biased diode when a transistor is turned off. For instance, in case of an Inverter with low input voltage, the NMOS is turned OFF and the PMOS is turned ON. The output voltage will be high because the PMOS is ON. Hence, the drain-to-substrate voltage of the OFF NMOS transistor is equal to the supply voltage. This results in a current leakage from the drain to the substrate through the reverse biased diode. The magnitude of the diode leakage current is dependent on the area of the drain diffusion and the leakage current density, which is set by technology. The sub threshold current is the drain-source of an OFF transistor. This is due to the diffusion current of the minority carriers in the channel for a MOS device operating in the weak inversion mode (sub threshold region). For instance, in case of an inverter with low input voltage, the NMOS is turned OFF and the output voltage is high. Even if the VGS is 0V, there is still a current flowing in the channel of the OFF NMOS transistor due to VDS potential of VDD. The magnitude of sub threshold current is a function of temperature, supply voltage, device size and process parameters. The process parameter that has a dominant effect on the sub threshold current values is the threshold voltage (VT).Reducing VT results in an exponential increase in the sub threshold current. Static power is also dissipated when current leaks between the diffusion layers and the substrate. For this reason, static power is often called leakage power

2.2.2 Dynamic power

Dynamic power is due to switching transient current and charging and discharging of load capacitances. Dynamic power is the power dissipated when the circuit is active. A circuit is active, any time the voltage on net changes due to some stimulus applied to the circuit. Because voltage on an input net can change without necessarily resulting in logic transition on the output, dynamic power can be dissipated even when an output net doesn't change its logic state.The below equation (1) shows the parameters for the dynamic power

$$P_D = (C_{diffusion} + C_{Fanout} + C_{Wire}) * a * F * V_{DD}2$$

…(1) Where , Pd = Dynamic power
Cdiffusion = Capacitance of the output transistors
CFanout = Capacitance of the output transistors of the next stage ,C wire= Capacitance of the interconnect wires , α = toggle rate,F = Frequency,Vdd = supply voltage,Following are the components to the Dynamic IR drop ,– switching (Load Capacitive) power – Short Circuit Power,– Internal Power

III power grid analysis

3.1 Static power grid analysis and flow

The main value of the static approach is its simplicity and comprehensive coverage. Since only parasitic resistance of the power grid is required the extraction task is minimized, and since every transistor or gate provides an average loading to the power grid the solution provides comprehensive coverage of the power grid. The main challenge of the static approach is accuracy. Local dynamic effects are not accounted for, neither are package inductance effects (L dI/dt), both of which may result in optimistic IR drop or ground.The Inputs to the Static IR drop analysis are net list and power grid of chip with transistor modeling information.
Static Power-Grid Sign-Off (PGS) typically consists of the following steps:
1. The parasitic resistance of the power grid is to be extracted.
2. A resistor matrix of the power grid is built.
3. An average current for each transistor or gate connected to the power grid is calculated.
4. The average currents are distributed around the resistance matrix, based on the physical location of the transistor or gate.
5. At every VDD I/O pin, a source of VDD is applied to the matrix.
6. A static matrix solve is then used to calculate the currents and IR drops throughout the resistance matrix. A static approach approximates the effects of dynamic switching on the power grid by making the assumption that de-coupling capacitances between VDD and VSS smooth out the dynamic peaks of IR drop or ground bounce. In this analysis the main advantage is required only parasitic resistance ,reducing the runtimes, comprehensive coverage and simplicity. But it has main challenge in accuracy.

3.2DynamicPower grid analysis and Flow :

Dynamic power dissipation occurs in logic gates that are in the process of switching from one state to another. During the act of switching, any internal capacitances associated with the gate's transistors must be charged, thereby consuming power. Of more significance, the gate must also charge any external (load) capacitances, which consist of parasitic wire capacitances and the input capacitances associated with any downstream logic gates.A dynamic power grid analysis requires that both resistance and capacitance of the power grid are extracted, and that a dynamic circuit simulation of the resistant RC matrix is completed. The main value of the dynamic approach is its accuracy. Since the results are based on circuit simulation, the IR drop and ground bounce results can be extremely accurate and take into account localized dynamic and package inductance effects.
Dynamic Power-Grid Analysis typically consists of the following steps:
1. The parasitic resistance and capacitance of the power grid is extracted.
2. The parasitic resistance and capacitance of the signal nets is extracted.
3. The design net list is extracted.
4. A circuit netlist is created from the extracted parasitic and netlists.
5. A circuit simulation is executed, based on a suite of simulation vectors, which simulates the transistors or gates dynamically switching and the effect of this switching on the power grid.
The advantage of Dynamic analysis is its accuracy and It takes into account localized dynamic and package inductance effects.
The main drawback of dynamic analysis is The parasitic extraction demands are high because you need to extract resistance and capacitance for the power grids and (as a minimum) the capacitance for the signal nets, The circuit simulation can contain a huge number of elements to be simulated, which strains the capacity of the circuit simulation engine. The vector set that is used to stimulate the simulation plays a dominant role in determining the quality of the output, if a comprehensive suite of vectors is not used, then the results will be questionable because sections of the power grid may not have been simulated.Finally, given the number of elements associated with a single power grid, a power grid analysis solution based on comprehensive dynamic simulation will not easily scale as design sizes continue to grow.

3.3 Electro Migration (EM)

Electro migration (EM), the mass transport of a metal due to the momentum transfer between conducting electrons and diffusing metal atoms, exists wherever current flows through metal wires. When electrons flow through wires on a chip, they collide with metal atoms, producing a force on the atoms that causes the wires to break over the chip's lifetime. When early ICs were returned from the field and examined under

a microscope, very fine "cracks" in the wires were found. The immediate fix was simple: make the metal wires thicker. Making wires thicker was easy when they were 10 microns wide, but it's not easy with today's 0.25-micron technology due to the difference in aspect ratio. The conditions necessary for EM to be a significant problem are bearing down on us with increasing speed and ferocity: aluminum wires, high current densities, long narrow wires, logic hazards, and high operating frequencies. These conditions now occur on both power grids and signal lines. More than ever, IC designers need tools that can find and help fix EM problems during the design stage before they become problems in silicon Electromigration may be modeled by the following equation, which is known as

Black's Equation:**t50=CJ-ne(Ea/kT)……**(2)

Where: t50 = the median lifetime of the population of metal lines subjected to electromigration;C = a constant based on metal line properties;J = the current density;n = integer constant from 1 to 7; many experts believe that n = 2;T = temperature in deg K;

k = the Boltzmann constant; and Ea = 0.5 - 0.7 eV for pure Al.

IV section

4.0 IR DROP AND EM ANALYSIS WITH THE REDHAWK TOOL

Apache's RedHawk power integrity solution is a full-chip cell-based power/ground design and verification product with integrated SPICE, addressing static and dynamic power integrity from early in the design flow through verification and sign-off.RedHawk is fully compatible with industry standard formats and easily drops into existing ASIC vendor and COT flows. RedHawk's physical power methodology, illustrated in Figure 3 is easily integrated into all three primary stages of chip design: Design Planning, Design Development, and Design Verification. The use of RedHawk in these design phases is described in the following dynamic analysis, depending on where you are in the design flow. The first method is based on .lib file data, which provides early feedback on dynamic hotspots. The second method is Apache Power Library (APL) based dynamic analysis, which provides transistor-level accuracy during verification, based on cell current waveforms in the characterized APL.

4.1.1 Design planning and Development

RedHawk enables early design analysis of static IR drop, and dynamic hotspot estimation using .lib-basedanalysis.ensure Figure 4 shows the design flow for running RedHawk-S, the static IR drop solution inputs and outputs.The following are the key steps in the static voltage drop analysis flow.

1. Prepare the design data and input files.

- Prepare the RedHawk technology file data on the IC process (tutorial.tech).

properprotectionfromcurrentspikes.

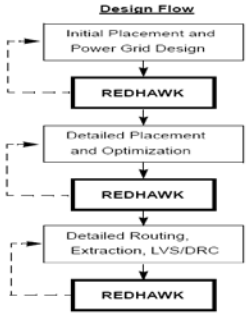

Figure 3 RedHawk in the Design process

4.2 Static Voltage Drop Analysis

- Prepare the pad cell name, pad instance name, or pad location file. (Tutorial. cell, tutorial.pad, and/or tutorial. loc file).
- Generate the STA output file for slews, timing windows, and clock instances (tutorial.sta) using the pt2timing.tcl script.
- Prepare the Global System Requirements (GSR) file (including references to .tech file, pad files, STA file, LEF files, DEF files, and LIB files) for static IR/EM and/or dynamic voltage drop analysis (tutorial.gsr).
- Import design data using GSR file (tutorial.gsr).

2. Perform power calculation from .lib cell data, or import power data if previously calculated.
3. Extract power grid (R network).
4. Perform static IR/EM analysis.
5. Generate and review maps and text reports of IR/EM results.
6. Perform "what-if" analysis and grid modification and optimization to fix areas of critical static IR drop.

RedHawk –S outputs include:

IR voltage drop contour maps• Electro-migration (EM) analysis

Power density and average current maps• Text report files of detailed static power, voltage, and currentdata

Warnings and violations reports

4.3 Dynamic Voltage Drop Analysis Flow

Figure 5 shows the design flow for running RedHawk-EV, the dynamic voltage drop solution.

The following are the key steps in the dynamic analysis flow.

1. Prepare the design data and input files.

- If RedHawk static IR drop analysis has been run, this step does not need to repeated, except to set specific dynamic run parameters in the GSR file.

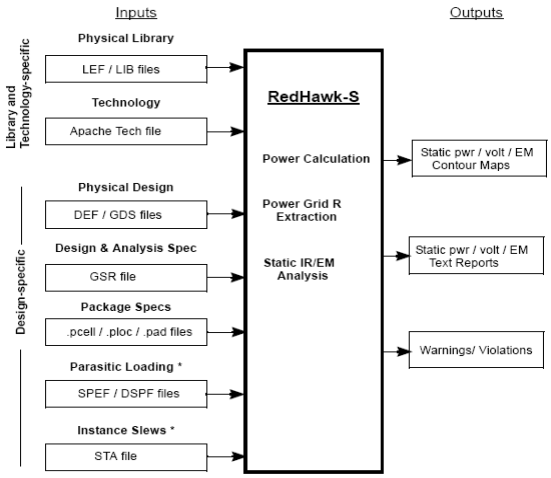

Figure 4 static IR drop inputs and outputs

- Prepare the RedHawk technology file data on the IC process.
- Prepare the pad cell name, pad instance name, or pad location file.
- Generate the STA output file for slews, timing windows, and clock instances using the pt2timing.tcl script.
- Prepare the Global System Requirements (GSR) file (including references to .tech file, pad files, STA file, LEF files, DEF files, and LIB files) for dynamic voltage drop analysis.-Import design data using GSR file

2. Prepare additional inputs required to run RedHawk-EV, in addition to those needed for static analysis.
- Timing windows and slews from STA (recommended)
- Extracted parasitic from SPEF or DSPF (recommended)
- Pad, wire bond/bump, and package R, L, C, K information
- Technology data - conductor thicknesses, dielectric thicknesses and dielectric constants
- SPICE model cards and library subcircuits. This is required to characterize the current waveforms in the Apache Power Libraries.
- SPICE subcircuits for all memories, I/Os, and IP blocks (optional)

3. Calculate detailed power distribution from .lib cell data, or import power data if previously calculated.
4. Extract power grid (RLC network).
5. Run APL (Apache Power Library) characterization, to obtain current profiles under typical corner conditions, Effective Series Resistance (ESR) for the power circuit and as well as decoupling capacitance and leakage current.
6. Perform dynamic voltage drop and peak current analysis.
7. Generate and review maps and text reports of dynamic analysis results.
8. Perform "what-if" analysis and optimize decap placement, make grid modifications and perform instance RedHawk-EV outputs include:• Dynamic voltage drop contour maps and power density contour maps.• Capacitance maps including decap effects.
• Report files.• ECO script to place and route environment. swapping to fix

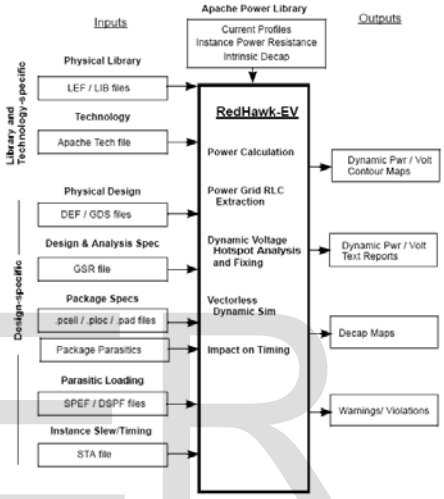

Figure 5 RedHawk-EV dynamic power analysis flow

4.4. IR DROPAnalysis generated flow

The following flow has been generated for the purpose of Static and Dynamic power analysis.

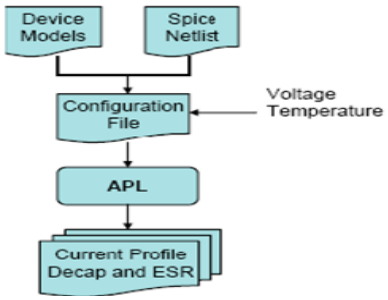

Figure 6 APL flow for extracting the current profile, decaps, and power circuit Effective Series Resistance for each cell

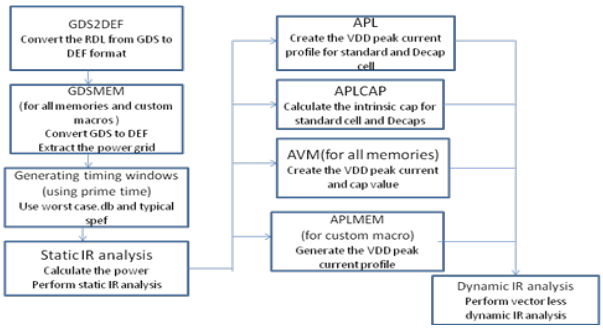

Figure 7 Generated Flow Diagram

SECTION V

5.0 STATIC AND DYNAMIC IR DROP ANALYSIS OF THE DIAGONAL POWER GRID DESIGN:

In this section we will discuses about the IR drop analysis of the Diagonal power grid and orthogonal power grid, comparison between the diagonal and orthogonal power grid. Full chip Diagonal power grid static and dynamic IR drop **analysis and power summary.**

5.1 Flow setting of the power grid analysis

When we analyze the IR drop analysis with Redhawk we required to mention the some of the parameters which is releted to the design. The main parameters are Frequency of the design, Library, Temperature, Functional corner, which spef's, operating voltage, data toggle rate, RAMS libs and standard cell libs.

The bellow is the operating condition parameters are Frequency = 940 MHz,Library = tt0p9v110C, Temp = 110C,TW = FuncTT

Spefs: typrc110c,Voltage: 0.90v,Activity Factor = 0.125,RAMS = lib_3.0.7,StdCells = lib_3.0.7,Design corners for APL (apache power library),IR = tt0p9v110c_0.9V_110C,EM = ff0p99v0c_0.99V_110C

5.2 Diagonal power grid IR Drop analysis

In this the top power grid metals are M9 and M8 which are the RDL layers. Metal M9 is routed diagonally with 45 degrees and M8 is routed horizontally. In present technology power consumption of the design is more. The problem is with the power delivery system. The IR drop is proportional to the average current consumed by the circuit in the chip. The L.di/dt drop is proportional to the time-domain change of the current due to the switching of the logic gates in the chip operation. The diagonal (M9) power grid is reducing the resistance and L di/dt effects. In this design M9 is routed with the 45 degrees to the M8 metal, in this case the no of vias between the M9 and M8 is increases and the effective resistance is less in the chip level. The power supply is connected from the M9 to the follow pins, in tile (block level) M7 is vertical power mesh and M6 is discontinued power mesh. In this analysis we considered the 4 blocks information in tile level and remaining blocks are block boxes, because of the run time and disk space, even we considered same information in orthogonal power grid for the comparison purpose.

The below table 1 shows the IR drop voltage information of the blocks in regions in the blocks. It will give the worst voltage drop information In the above table listed three designs x1, x2 and x3. The maximum IR drop in the design x1 is 140mv. The design supply voltage is 0.9v. This drop is the 15.56% of the supply voltage. The drop in the design we divide into the range like the percentage of the instances in the design greater than the divide range which is easy to study in the respective range according to requirement. The design x1 having the %of instances is greater than 13% is 0.09%, similary greater than 12 and 10% as shown in table. The no if instances in the design x1 are greater than 13% is 146, table gives detail information for different range.

the design x2 the maximum IR drop is 131.5mv, the

Redhawk tool will analyze the IR drop is cell based this will indicate the worst IR drop at cell node. In the x2 design the maximum drop is 14.6%. The table shows the percentage instances and number instances.

The design x3 has a maximum voltage drop 113.20mv and 12.58% in the supply voltage. The percentage of instances greater than 13% is 0, this block contain the less IR drop compare to the other

Block name	IRdrop (mv)	Irdrop (%)	%inst > 13%	%Inst >12 %	%Inst >10 %	Noinst >13 %	Noinst >12 %	No Inst >10%
x1	140.00	15.56		5.75	46.34	146	9374	75552
x2	131.50	14.61	0.01	0.57	10.68	9	460	8616
x3	113.20	12.58	0.00	0.11	12.57	0	298	33956

Table 1 Diagonal IR drop information of the blocks

blocks.The contour map of the IR drop of the diagonal power grid design as shown in below fig 8 The red hawk will give the map of the voltage drop in the design with the different colors. The color range can be changed in the redhawk by user requirement. In the above map the red color is shows the IR drop

greater than 12%. Similarly we can set the different colors for different range generally red will for high IR drop.The Diagonal power grid design have very less red spots in the design, with the help of map we can directly go to that particular region easy to identify the

In this the top RDL layers are M9 and M8. In this case chip level the power grid M9 and M8 are orthogonal to each other. The Layer M9 is routed vertically and M8 is horizontally. In block level M7 is the power mesh and M6 is power mesh with discontinues. The bottom layers are stacked vias up to the follow pin.

The no of vias between the M9 and M8 is less compared to the Diagonal power grid , the resistance is more and also the length of the layers are more compared to the diagonal.The table 2 shows the IR drop information of the different blocks.

the Orthogonal power grid analysis same block as considered to the diagonal power grid. The top layer routing is different. The diagonal power grid analysis the design x1 has the maximum voltage is 148.40mv and the percentage of voltage drop is 16.49mv from the supply voltage. The instance percentage greater than 13% is 0.51% and the number instances are 832.The design x2 has the 137.43mv maximum IR drop which is the 15.27% in the supply voltage. The percentage instances greater than 13% is 0.02%. The design x3 has the maximum of 119.16mv and 13.24% of the supply voltage. The table indicates the information about the three blocks of the maximum voltage drop and corresponding design percentage instances.

Table2 Orthogonal power grid IR drop Information

Block name	IRDrop (mv)	IRdrop (%)	%inst >=13	%Inst >=12	%Inst >=10	Nr inst >=13%	Nr Inst >=12%	Nr Inst >=10%
x1	148.40	16.49	0.51	7.67	49.74	832	12509	81095
x2	137.43	15.27	0.02	0.04	11.58	18	840	9343
x3	119.16	13.24	0.01	2.31	14.96	27	6240	40412

5.3 Comparison between the Diagonal and Orthogonal power grid

The above information gave the IR drop results with different grid structure. In the diagonal power grid the IR drop is less compare to the orthogonal because of the resistance and L.di/dt effects, the less resistance is due to the more parallel vias in diagonal compare to the orthogonal. In the Diagonal grid the current loop path is less compared the orthogonal due to this the L.di/dt effect is less.In above cases the design x1 has 8mv less IR drop in the diagonal

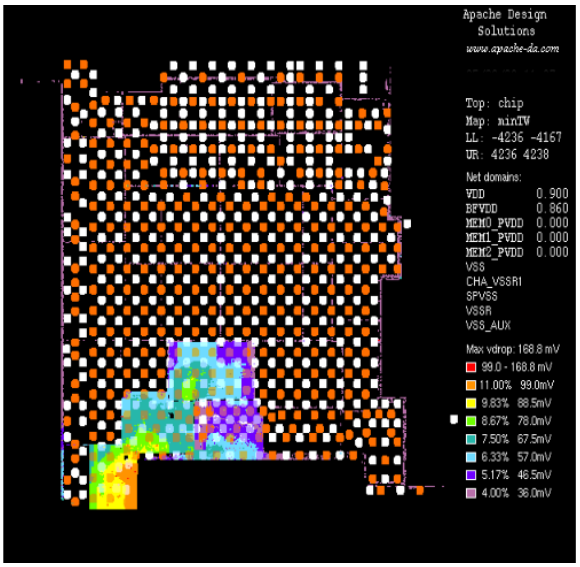

Figure 8 shows the IR drop of the Diagonal power grid design

compared to the orthogonal and also the percentage and the number of instance is come down from higher voltage drop to lower drop region.The design x2 benefited the 6mv compared to the orthogonal power grid. The number instances greater than 10%is come down form 9343 to 8616.Similarly the design x3 also has 6mv less compare to the orthogonal power grid. The overall from the 3 design an average

6 to 8mv is less in the diagonal grid. In the IR drop maps also the red areas is more in orthogonal power grid compared to the Diagonal. From the above analysis we implemented the diagonal power grid in chip level power grid to reduce the IR drop problems

5.4 Defining Pad and Package Parameters

Before performing static IR drop and EM analysis, the pad, package wire bond or flip-chip bumps and associated electrical package parameters must be defined.Three types of package models are available, simple models in which all power pads have the same RLC values and all ground pads have the same RLC values. More complicated package modeling, in which different values can be assigned to each pad, are provided by a spice subcircuit model or an S-parameter model. These three types of models are described in the following sections.

5.4.1 Simple Package RLC Model:A simple package circuit model representation in RedHawk is shown in Figure.9 Package parasitic represent RLC values associated with the package substrate itself. The wire bond represents the bond wire (lead frame to bond pad connection) parasitic. For Flip Chip designs, where there is no lead frame, this can be included as a part of package parasitic. Pad wire

parasitic represent the parasitic of the pad (or bump) wire routing (bond pad/bump to I/O pad cell connection). If this routing is already included in the DEF, RedHawk extracts the information automatically; you do not need to specify these values.

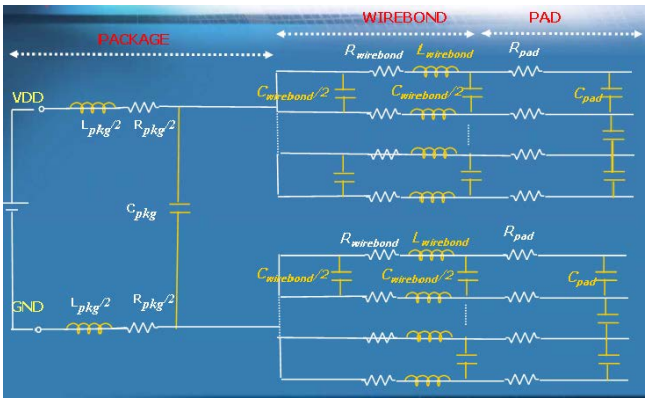

Figure 9 simple package RLC model

The pad, wire bond or flip-chip bump, and package parasitic are typically specified in the Redhawk.tech file. The units used for the package TCL commands are: R in Ohms, C in picoFarads, and L in PicoHenrys.

The following three TCL commands define simplified lump models for all pad RC, wire bond/ bump RLC, and package RLC circuits, respectively.

Setup pad [-power | -ground] [-r <Rohm's> | -c <C_pF>]

Setup wire bond [-power | -ground][-r <Rohm's> | -l <L_pH> | -c <C_pF>]

Setup package -r <Rohm's> -l <L_pH> -c <C_pF>]

Where(L,C&R are the specified values in pico henrys,pico farad&ohms respectively

-Power -ground: selects which P/G net to define

To specify individual bump/pad RLC values, in "Pad Location File (*.ploc)". If you need a more accurate use spice package sub circuit for the design.

To set up your package parameters such that you can easily look at the effects of different package designs on power integrity, after extraction you can use the TCL command.

'Setup pss', which defines PLOC and package subcircuit files to be used in simulation, using the follow syntax:

Setup pss -pad_file <filename> -subckt <pss_ckt_name>

Where

-pad_file <filename>: specifies a PLOC pad definition file that must have a .ploc extension and be in PSS PLOC format.

-subckt <pss_ckt_name>: specifies the spice package subcircuit file After running RedHawk with one set of PLOC and package subcircuit files, you can then modify one or both of the files, rerun the 'setup pss' command, and then rerun RedHawk to see the effects of the new package data.

5.5 Static IR drop Analysis

The following are the stpes for the static IR drop

1. Prepare design data files 2. Import design data using the automated setup script or the GSR file 3. Perform power calculation 4. Perform power grid extraction for R network..5. Evaluate power/ground grid weakness.6. Define pad and package constraints.7. Perform static IR voltage drop and EM analysis.8. Review static IR/EM summary reports and evaluate what other information is needed from the analysis.9. Explore solutions to reduce excessive static IR drop with the Redhawk power grid Fixing anfd Optimization toolSome of the commands are used during static IR drop Analysis:(setup design,perform pwrcalc ,perform extraction -power -ground -c –l,perform analysis –static)

The following results shows the static IR drop results of the some the tiles

5.5.2 Power summary of the design

The redhawk will calculate the power of the design during analysis by performing power calculation. As shown in below Power of different frequency (MHz) domain in Watt: Frequency total_pwr leakage_pwr internal_pwr switching_pwr %_total_pwr

9.3985e+02 4.0182e+01 2.8164e+00 2.2860e+01 1.4505e+01 8.8776e+01
6.0024e+02 1.8228e+00 1.8201e-01 1.0725e+00 5.6829e-01 4.0271e+00
4.8828e+02 1.9378e-01 2.5823e-02 1.1006e-01 5.7905e-02 4.2814e-01

Power of different Vdd domain in Watt:

Vdd_domain total_pwr leakage_pwr Internal_pwr switching_pwr %_total_pwr
VDD (0.9V) 4.4755e+01 3.3513e+00 2.5601e+01 1.5803e+01 9.8879e+01

Power of different cell types in Watt:

cell_type total_pwr leakage_pwr internal_pwr switching_pwr %_total_pwr
Combinational 1.8396e+01 1.6648e+00 6.1896e+00 1.0541e+01 4.0642e+01
latch_and_FF 1.6516e+01 1.0029e+00 1.3759e+01 1.7544e+00 3.6491e+01
Memory 7.9349e+00 6.4625e-01 4.4691e+00 2.8196e+00 1.7531e+01
clocked_inst 2.3755e+00 4.6938e-02 1.4854e+00 8.4314e-01 5.2482e+00

Decap 3.9921e-02 3.9921e-02 0.0000e+00 0.0000e+00 8.8199e-02

Total chip power, 45.262 Watt including core power and other domain power.Total clock network only power, 7.0583 Watt. Total clock power including clock network and FF/latch clock pin power, 20.905 Watt.In above report indicating the power consumption design for at all frequencies if the design have one more. It categorize the total power consumption at part particular frequency and from that what is leakage power , internal power and switching power ,percentage of the total consumption of the chip.In this at 940 MHz total power is 40.18 watts, which is 88.77% of the total power remaining power is consumed by other frequency.It will also reports the power consumption of the different voltage domains, the blocks in the design's operated in two voltage modes one is 0.9v and another is art 1.1v, in this we not reporting the 1.1v ,in design we have only one sub blocks operated at 1.1v.The redhawk will also report the power consumption of the each cell , as shown in above it will reporting the all combinational cell, latches and flip-flops ,memories, clock cells and decaps separately.

5.6 Electro migration Analysis

During the static IR drop analysis the redhawk will also reports the EM information.

In EM report file, RedHawk reports all METAL EM violations using the following format.

#Layer #End-to-end_coordinates #EM_Ratio #Net #Width

METAL4 (4905.670, 3398.849 4905.670, 3400.562) 469.016% VDD 25.000

RedHawk calculates the actual current density as follows:

Actual I density = (Current/Eff_Width) = 219.664 /(25-0.016) = 8.7922 mA/u

And the EM limit for METAL4 in the tech file is defined as 1.874 mA/u. RedHawk calculates the EM_Ratio using the following equation.

EM_Ratio = 100 * (Actual density of current) / (EM limit in tech file).

Therefore

EM_Ratio = 100 * 8.7922 / 1.874 = 469.2

For VIAs, RedHawk reports the EM violations in the following format:

#Via_name #x-y_coordinates #EM_Ratio #net

via via3Array_87 (3154.820,893.390) 172.29% GND

The EM_ratio of a VIA layer is calculated as follows (percentage):

EM_Ratio = (Current through the VIA)*100 /(EM limit)

EM violations are mostly caused by weak power grid connections feeding current to high power-consuming regions or blocks in the design. If this is the case, increasing the metal width to reduce the current density is a typical solution. Similarly, for a via EM violation, you can increase the number of vias to fix potential EM issues. You also can provide additional straps for the current supply, thereby reducing the current-per-strap value. Layer switching is another option; typically, upper metal layers in the technology have higher current driving capability (due to greater thickness). So you can use these layers for designing the major power grids (grids with higher current flow) in the design. You can use the what-if and Fix and Optimize capabilities to modify the grid for fixing EM violations. Using this method you can edit any existing strap or add any new straps or vias.

TILE	IR(mv)	IR%
Core/zzz_1	176.2	19.57
Core/zzz_2	47.5	5.27
Core/zzz_3	44.3	2.92
Core/zzz_4	35.1	3.9
Core/zzz_5	33.9	3.76
Core/zzz_6	28.8	3.2
Core/zzz_7	27.5	3.05
Core/zzz_8	20.5	2.77
Core/zzz_9	13.4	1.55
Core/zzz_10	9.5	1.05
Core/zzz_11	8.7	.96
Core/zzz_12	140.04	15.60
Core/zzz_13	119.7	13.3
Core/zzz_14	115.2	12.9
Core/zzz_15	102.6	11.4

Table 3 Static voltage drop reports

5.6.1 Signal EM Analysis

Signal EM analysis should estimate the Iavg, Irms, and Ipeak for every wire in the design, especially those belonging to the clock tree network, and compare them against their respective EM limits. The signal EM flow in RedHawk estimates these different current values based on cell design parameters. RedHawk analyzes signal EM for all wires in a design - both inside cells (intracell) and between cells (inter-cell). The average current flowing in every wire (Iavg) is estimated from the capacitive load seen at the output of each cell, its operating frequency, its supply voltage and toggle rate (which is defined as

2.0 or 200% for clock pins). Iavg = f (capacitive load, frequency, toggle rate, supply voltage) since the current flowing in a signal net is usually bi-directional; the true average current is usually very small. Therefore in RedHawk a rectified average current is calculated.

5..6.2 EM Results of the power network

In the design the EM ratio greater than 100% that reports the violation on that metal.The following reports show some of the em violation's in the design

#Layer#end-to-end-coordinates EM_Ratio #net #width

Metal1 (3996.090, 4659.480, 3998.484, 465980) 153.83% VSS 0.23

Metal1 (3995.98, 4659.480, 3996.09, 4660.61) 129.255% VDD 0.23

Metal1 (3993.94, 46660.61, 3995.98, 4660.64) 128.248% VDD 0.23

Metal1 (3980.34, 4660.61, 3982.284, 4660.614) 100.373% VDD 0.23

The below Map shows the Metal1 EM violation's in the design In the map the red color shows the EM ratio is greater than 100%, the metal violated the EM rule. This is due to the improper power network, shorts in the power grid metal and vias missing between the metal.

5.7 Dynamic IR Drop Analysis

Redhawk will analyze the dynamic IR drop by considering the peak current in the t profile design. The dynamic IR drop effects involving temporal relationships between switching events (of cells, clocks, memories, IP, and I/O buffers) and the impact that capacitance and inductance have on full-chip power integrity. The Inputs required to the dynamic

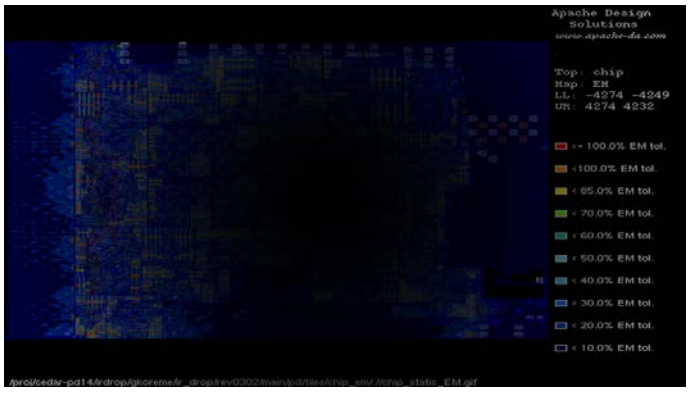

Figure 10 Metal1 EM violation's in the design

IR drop analysis

• LEF files for cell library, including standard cells, memories, and I/Os
• Flat or hierarchical DEF files
• Synopsys .lib library files
• Apache .tech technology file - conductor and via resistance, dielectric thicknesses and dielectric constants, EM current density limits
• Pad instance, pad cell, or pad location files
•Apache Global System Requirements (GSR) file, containing information on toggle rates, frequency, clock roots, default slews, and block power
• Timing windows and slews from STA (recommended).
• Extracted parasitic from SPEF or DSPF (recommended)
• Pad, wire bond/bump, or package RLC information (recommended)
• VCD vector file (recommended if available)
• SPICE sub circuits for all memories, I/Os, and IP blocks (optional)
• GDSII for memories, I/Os, and IP blocks (optional)

5.7.1 Method's of Dynamic IR drop analysis with Redhawk

There are several methods of vectorless and VCD-driven dynamic voltage drop analysis available in RedHawk. The chosen method of performing dynamic voltage drop analysis depends primarily on whether a VCD file is available, and if so, the quality of the VCD information. The goal is to use the best switching information available to construct a realistic switching scenario with the information available. Available methods for performing dynamic analysis are summarized in the Figure 11. diagram following. To aid in deciding what type of dynamic analysis to perform, key characteristics of vectorless, VCD-driven vectorless, and VCD dynamic analysis are presented following the diagram.

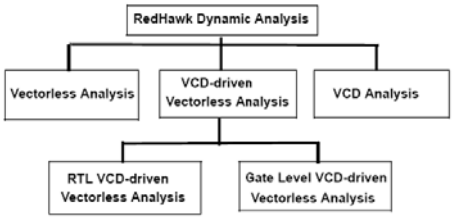

Figure 11 Types of Redhawk Dynamic Analysis

Table 4. Dynamic IR drop Reports

The below are the dynamic voltage drop block wise details

TILE	IR (mv)	IR %
Core/zzz_00	280.3	31.1444
Core/zzz_01	284.4	31.6
Core/zzz_02	262.7	29.1889
Core/zzz-03	198.5	22.0556
Core/zzz_04	304.6	33.8444
Core/zzz_05	123.7	13.7444
Core/zzz_06	515.9	57.3222
Core/zzz_07	205.1	22.7889
Core/zzz_08	254.6	28.2889
Core/zzz_09	177.7	19.7444
Core/zzz_10	250.2	27.8
Core/zzz_11	209.3	23.2556
Core/zzz_12	258.2	28.6889
Core/zzz_13	209.7	23.3
Core/zzz_14	213.7	23.7444
Core/zzz_15	226.6	25.1778
Core/zzz_16	216	24.00
Core/zzz_17	413.5	45.9444
Core/zzz_18	93.5	10.3889
Core/zzzz_19	191.8	21.3111
Core/zzz_20	73	8.11111
Core/zzz_21	246.1	27.3444
Core/zzz_22	179.9	19.9889
Core/zzz_23	370.1	41.1222
Core/zzz_24	144.9	16.1
Core/zzz_25	369.7	41.0778
Core/zzz_26	199.6	22.1778
Core/zzz_27	382	42.4444
Core/zzz_28	188.3	20.9222
Core/zzz_29	370.3	41.1444

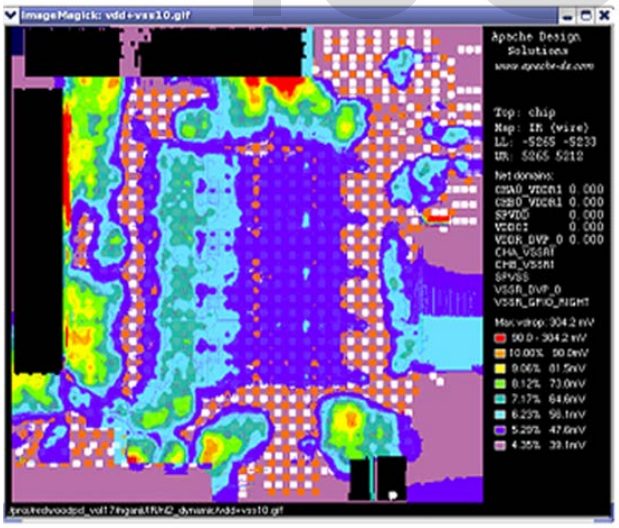

Figure 12 VDD and VSS Dynamic IR drop map

Redhawk will analyze the VSS, VDD together and separately, we need to make sure that there is no short between the VSS and VDD.The redhawk will also give the contour maps of the drops as shown in below this map is combination of both VSS and VDD In the above fig the worst drops are at the outer region, in the flip chip design the signal and power connection are through the bumps. In the design where the power bump pitch is more in that region the drop is more ,the pitch is more in some regions because of the in between the power bumps the signal bumps are present. In the fig the regions with red color shows the more IR drop compared to the other regions.

Acknowledgement: The authors would like to thanking to AMD division engineers of Hyderabad extending their help for this test case.

6. Conclusion:

As device scaling progressed and the greater number of components was integrated onto a single die, on-chip power dissipation began to produce significant economic and technical difficulties. The problem of EMI created due to dynamic power dissipation in Ldi/dt effect which is the problem is basic power delivery system. EM interference problem is reduced If the power network is good the amount of voltage is with in the limit. we discussed qualitative treatment of IR drop and how the diagonal power grid reduce the voltage drop effects compare to the orthogonal power grid. The resistance of the power grid circuit will reduced by the diagonal power grid routing, we control the voltage drop effects due to average current flowing. The diagonal routing also reduce the L.di/dt effect by shortest path loop, compare to the orthogonal routing. We discussed Red hawk physical power methodology, the inputs and outputs of the static and dynamic analysis. The IR drop flow analysis with the redhawk tools with different stages, the generic flow and in each stage we discussed about step and corresponding stage details. we analyze the IR drop analysis with diagonal and orthogonal power grid design. The comparison of the diagonal and orthogonal voltage drop results In this conclusion is the diagonal power grid has less voltage drop compare to the orthogonal. In the diagonal routing the number of parallel vias are more compare to the orthogonal in between the M9 and M8 metal .

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16 Power Optimization within Nanometer Designs www.tayden.com/publications/Power%20Optimization%20within%20Nanometer%20Designs.pdf

17 Power Reduction Techniques for Nanometer Designs Targeting Mobile Applications www.solvnet.synopsys.com

18 Analysis of IR-Drop Scaling with Implications for Deep Submicron P/G Network Designs http://www.ece.ucsb.edu/Faculty/Banerjee/pubs/ISQED_IRDrop_2003.pdf

19 Power Supply Noise Aware Floorplanning and Decoupling Capacitance Placement http://delivery.acm.org/10.1145/840000/835431/14410489.pdf?key1=8354

20 Cadence User guide